REMARKS

Prior to entry of this amendment, claims 1, 3-20 and 23-28 are pending. By this amendment, claims 3-5, 7-9, 14 and 18 are amended. No new matter is added.

Claims 1, 3-20 and 23-28 are presented for examination.

Favorable reconsideration of this application is respectfully requested in view of the foregoing amendments and following remarks.

Claim Rejections Under 35 U.S.C. § 112,

In the Office Action mailed December 1, 2004, claims 3-20 and 25-28 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 3-5, 7-9, 14 and 18 have been amended responsive to this rejection. If any additional amendment is necessary to overcome this rejection, the Examiner is requested to contact the Applicant's undersigned representative at the telephone number listed below.

Claims 1, 3-20 and 23-28 Recite Patentable Subject Matter

Claims 1, 3-20 and 23-28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,034,563 to Mashiko (hereinafter, "Mashiko"). It is noted that claims 3-5, 7-9, 14 and 18 have been amended. To the extent that the rejection remains applicable to the claims currently pending, the Applicants hereby traverse the rejection, as follows.

Independent claims 1 and 8 recite a semiconductor device, including, among others, features wherein (1) a high-threshold N-channel type MIS field effect transistor is connected to a pseudo high-potential power supply line VDDV, (2) a back gate of a low-threshold P-channel type MIS field effect transistor of a load circuit is connected to the pseudo high-potential power supply line (VDDV), and (3) a ground terminal (second

power supply terminal) of the load circuit is connected to a real low-potential power supply line GND. Applicant respectfully submits that these features of claims 1 and 8 are neither disclosed nor suggested by Mashiko.

Applicant notes that in claims 1 and 8, according to features (1) – (3) above, (a) existing standard cells can be used to constitute the semiconductor integrated circuit device, (b) a twin-well process less costly than a triple-well process can be used for the fabrication of the circuit device, and (c) the layout area can be reduced compared with the prior art semiconductor integrated circuit devices. Applicant respectfully submits that these advantages (a) - (c), provided by the claimed invention, cannot be obtained by the device of Mashiko.

Independent claim 9 recites a semiconductor device, including, among other features, a high-threshold N-channel type MIS field effect transistor and a waveshaping circuit. The waveshaping circuit receives an output signal of a level conversion circuit, and performs waveshaping such that an output signal of the waveshaping circuit rises slower than a control signal. The high-threshold N-channel type MIS field effect transistor of claim 9 exhibits source-follower characteristics, so that the output signal of the waveshaping circuit rises slower than the control signal.

In contrast, Mashiko discloses a high voltage generating circuit 13 and a low voltage generating circuit 14 which are used to apply a high potential V_{PP} or a low potential V_{BB} to the gate of a P-channel type MOS field effect transistor Q1. Because MOS field effect transistor Q1 is a P-channel type MOSFET and not an N-channel type MOSFET, MOS field effect transistor Q1 does not display source-follower characteristics. Thus, it is respectfully submitted that the circuit of Mashiko cannot and does not provide the waveshaping characteristics of the invention as recited in claim 9.

To establish prima facie obviousness of a rejected claim, the applied art of record must teach or suggest each feature of a rejected claim. *See M.P.E.P. §2143.03.* As explained above, Mashiko neither discloses nor suggests each and every feature recited in independent claims 1, 8 and 9. Accordingly, Applicants respectfully submit that Mashiko neither anticipates nor renders obvious the present invention as recited in independent claims 1, 8 and 9.

For at least the reasons set forth above, Applicants respectfully submit that independent claims 1, 8 and 9 are patentably distinct over Mashiko and in condition for allowance.

Each of claims 3-7, 10-20 and 23-28 depends from one of claims 1, 8 and 9. Therefore, Applicants respectfully submit that claims 3-7, 10-20 and 23-28 are allowable for the same reasons as claims 1, 8 and 9, as well as for the additional subject matter recited therein.

Accordingly, withdrawal of the rejection of claims 1, 3-20 and 23-28 under 35 U.S.C. § 103(a) is respectfully requested.

Conclusion

For all of the above reasons, it is respectfully submitted that claims 1, 3-20 and 23-28 are in condition for allowance and a Notice of Allowability is earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300 referencing client matter number **100021-00133**.

Respectfully submitted,

Arent Fox, PLLC

Michele L. Connell
Registration No. 52,763

Customer No. 004372
1050 Connecticut Ave., N.W., Suite 400
Washington, D.C. 20036-5339
Telephone No. (202) 857-6104
Facsimile No. (202) 857-6395

MLC:sg